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MC68328
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Product Brief
Integrated Portable System Processor—DragonBall™

As the portable consumer market grows in full speed, the system requirements are becoming more rigorous than ever. Minimum components, small board space, low power consumption, and low system cost are several minimum criteria to a successful product. To address these needs, Motorola designed a new processor MC68328 DragonBall™. By providing 3.3V, fully static operation in an efficient package, the MC68328 delivers cost-effective performance to satisfy the extensive requirements of today's portable consumer market.

The MC68328 (shown in Figure 1) is the first integrated processor of the 68K Family to include a LCD controller, which demonstrates Motorola's focus on the portable market. With addition to the LCD controller, MC68328 provides key features that are suitable for many portable applications. Modules like RTC, PWM, Timers, Master SPI, Slave SPI, UART, and the System Integration Module (SIM28) facilitate the system engineer with more flexibility and resources to design efficient and innovative products.

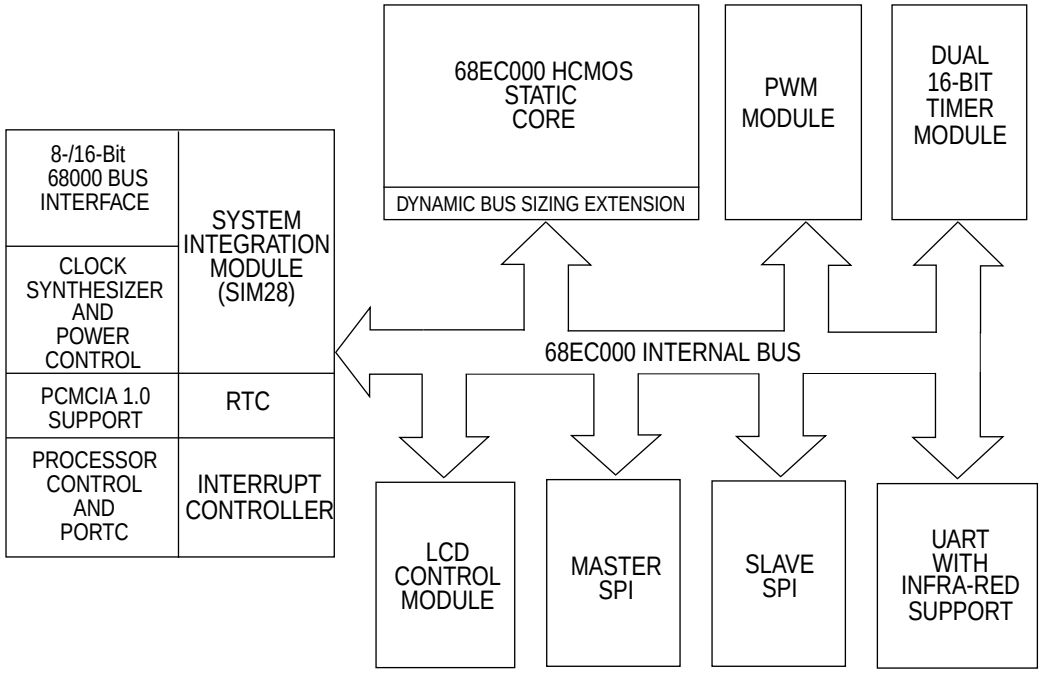

Figure 1. MC68328 Block Diagram

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KEY FEATURES

The primary features of the MC68328 are as follows:

- Static 68EC000 Core Processor—Identical to MC68EC000 Microprocessor
  - — Full Compatibility With MC68000 And MC68EC000
  - — 32-Bit both External and Internal Address Bus capable of addressing 4GB Space
  - — 16-Bit On-Chip Data Bus For MC68000 Bus Operations
  - — Static Design Allows Processor Clock To Be Stopped Providing Dramatic Power Savings
  - — 2.7 MIPS Performance At 16.67-MHz Processor Clock
- External M68000 Bus Interface with Dynamic Bus Sizing for 8-bit and 16-bit Data Ports
- System Integration Module (SIM28), Incorporating Many Functions Typically Relegated to External Array Logic, such as:
  - — System Configuration, Programmable Address Mapping
  - — Glueless Interface to SRAM, EPROM, FLASH Memory
  - — Sixteen Programmable Peripheral Chip Selects With Wait State Generation Logic
  - — Interrupt Controller with 13 flexible inputs
  - — Programmable Interrupt Vector Response For On-Chip Peripheral Modules
  - — Hardware Watchdog Timer
  - — Software Watchdog Timer
  - — Low-Power Mode Control
  - — Up to 78-Bit Individually Programmable Parallel I/O Ports
  - — PCMCIA 1.0 Support
- UART
  - — Support IrDA Physical Layer Protocol
  - — 8 Bytes FIFO on Rx and Tx
- Two Separated Serial Peripheral Interface Ports (Master and Slave)
  - — Support For External POCSAG Decoder (Slave)
  - — Support for Digitizer from A/D Input or EEPROM (Master)
- Dual Channel 16-Bit General Purpose Counter/timer
  - — Multimode Operation, Independent Capture/Compare Registers
  - — Automatic Interrupt Generation
  - — 240-ns Resolution At 16.67-MHz System Clock
  - — Each Timer Has An Input And An Output Pin for Capture and Compare
- Pulse Width Modulation Output For Sound Generation
  - — Programmable Frame rate
  - — 16 Bit programmable
  - — Supports Motor Control
- Real Time Clock
  - — 24 Hour Time
  - — One Programmable Alarm
- Power Management
  - — 5 V or 3.3 V Operation
  - — Fully Static HCMOS Technology
  - — Programmable Clock Synthesizer for Full Frequency Control
  - — Low Power Stop Capabilities
  - — Modules Can Be Individually Shut-down
  - — Lowest Power Mode Control (Shut Down CPU and Peripherals)

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- LCD Control Module
  - — Software Programmable Screen Size To Support Single (Non-Split) Monochrome/ STN Panels
  - — Capable Of Direct Driving Popular LCD Drivers/Modules From Motorola, Sharp, Hitachi, Toshiba etc.
  - — Support Up To 4 Grey Levels
  - — Utilize System Memory as Display Memory
- IEEE 1149.1 Boundary Scan Test Access Port (JTAG)
- Operation From DC To 16.67 MHz (Processor Clock)
- Operating Voltages of 3.3V ± 0.3V and 5V ± 0.5V
- Compact 144-Lead Thin Quad Flat Pack (TQFP) Package

SYSTEM INTEGRATION MODULE

The MC68328 system integration module (SIM28) consists of several functions that control the system start-up, initialization, configuration, and the external bus with a minimum of external devices. The memory interface allows the user to interface gluelessly with the popular SRAM, EPROM as well as PCMCIA 1.0 memory cards, with the assistance of chip-select logic, wait states can be programmable. The hardware and software watchdog timers help the user to do system protections. The interrupt controller accepts and resolves the priority from internal modules and external generated interrupts and also handles the masking and wake-up selection control for power control. The low-power logic can be used to control the CPU power dissipation by altering the frequency or stopping it. The SIM28 is also capable of configuring the pin to allow the user to select either dedicated I/O or parallel I/O. This feature helps to increase the number of available I/O ports by reclaiming when the dedicated function is not in used

System Configuration

The MC68328 system configuration logic consists of a system control register (SCR) and which allows the user to configure operation of the following major functions:

- System Status and Control Logic
- Register Double Mapping
- Bus Error Generation Control
- Protecting the module control registers from access by user programs

VCO/PLL Clock Synthesizer

The clock synthesizer can operate with either an external crystal or an external oscillator for reference, using the internal phase-locked loop (PLL) and voltage-controlled oscillator (VCO), or an external clock can directly drive the clock signal at the operating frequency.

Chip Select Logic

The MC68328 provides sixteen programmable general purpose chip-select signals. For a given chip-select block, the user may choose whether the chip-select allows read-only, or both read and write accesses, whether the chip-select should match only one function code value or all values, whether a $\overline{\text{DTACK}}$ is automatically generated for this chip-select, and after how many wait states (from zero to six) the $\overline{\text{DTACK}}$ will be generated.

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External Bus Interface

The external bus interface handles the transfer of information between the internal 68EC000 core and the memory, peripherals, or other processing elements in the external address space. It consists of a 16-bit 68000 bus interface for internal and a selectable 8-bit or 16-bit interface to outside.

Interrupt Controller

The interrupt controller accepts and prioritizes both internal and external interrupt requests and generates a vector number during the CPU interrupt acknowledge cycle. Interrupt nesting is also provided so that an interrupt service routine of a lower priority interrupt may be suspended by a higher priority interrupt request. The on-chip interrupt controller has the following major features:

- Prioritized Interrupt Sources (Internal and External)
- A Fully Nested Interrupt Environment
- Programmable Vector Generation
- Interrupt Masking
- Wake-up interrupt Masking

Parallel General-Purpose I/O Ports

The MC68328 supports up to 78-bit general-purpose I/O ports, which can be configured as general-purpose I/O pins or as dedicated peripheral interface pins of the on-chip modules.

Each port pin can be independently programmed as general-purpose I/O pins, even when other pins related to the same on-chip peripheral are used as dedicated pins. Even if all the pins for a particular peripheral are configured as general-purpose I/O, the peripheral will still operate normally, although this is only useful in the case of the RTC and timer modules.

Software Watchdog

A software watchdog timer is used to protect against system failures by providing a means to escape from unexpected input conditions, external events, or programming errors. Once started, the software watchdog timer must be cleared by software on a regular basis so that it never reaches its time-out value. Upon reaching the time-out value, the assumption is made that a system failure has occurred, and the software watchdog logic resets or interrupts the 68EC000 core.

Low-Power Stop Logic

Various options for power-saving are available: turning off unused peripherals, reducing processor clock speed, disabling the processor altogether or a combination of these.

A wake-up from low-power mode can be achieved by causing an interrupt at the interrupt controller logic which runs throughout the period of processor low-power. Selectable interrupt will cause a wake-up of the EC000 core followed by processing of that interrupt.

The on-chip peripherals can initiate a wake-up; for example, the timer can be set to wake-up after a certain elapsed time, or number of external events.

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LCD Controller

- Interfaces with Monochrome STN LCD Modules
- Up to 4 Levels of Gray Scale through Frame Rate Control
- Utilize system RAM for display memory
- Screen Refresh through DMA

UART and Infra-red Communication Support

The UART supports standard asynchronous serial communications at normal baud rates and is compatible with HPSIR/IrDA Physical Communication Protocol

Real Time Clock

Real Time Clock in MC68328 is driven by a 32.76KHz/38.4kHz Crystal which is the same as the Clock Synthesizer Clock source. It provides interrupt for alarm.

JTAG Test Access Port

To aid in system diagnostics the MC68328 includes dedicated user-accessible test logic that is fully compliant with the IEEE 1149.1 standard for boundary scan testability, often referred to as JTAG (Joint Test Action Group).

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ORDERING INFORMATION

Table 1 identifies the packages and operating frequencies available for the MC68328.

Table 1. MC68328 Package/Frequency Availability

Package Type	V_{CC}	Frequency (MHz)	Temperature	Order Number
144-Lead TQFP	5V 3.3V	16.67 16.67	0°C to 70°C	MC68328

The documents listed in Table 2 contain detailed information on the MC68328. These documents may be obtained from the Literature Distribution Centers at the addresses listed at the bottom of this page.

Table 2. Documentation

Document Title	Order Number	Contents
MC68328 User's Manual	MC68328UM/AD	LDC Stocking est. 2Q95
M68000 Family Programmer's Reference Manual	M68000PM/AD	M68000 Family Instruction Set

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